What is claimed is:

1. A method of forming a semiconductor device, the steps comprising:

forming a silicon dioxide layer on a semiconductor substrate;

forming a silicon nitride layer on said silicon dioxide layer;

forming isolation trench regions in said semiconductor substrate;

removing said silicon nitride layer;

first implantation of dopant through said silicon dioxide;

second implantation of dopant through said oxide to form wells; and

removing said implanted oxide layer and forming a gate dielectric layer over said

semiconductor substrate.

- 2. The method of forming a semiconductor device according to claim 1, wherein said silicon dioxide layer thickness is approximately about 25 °A 120 °A.
- 3. The method of forming a semiconductor device according to claim 1, wherein said first implanted dopant comprises n- or p- type ions.
- 4. The method of forming a semiconductor device according to claim 3, wherein said first implanted n- type dopant is As<sup>+</sup> or P<sup>+</sup> ion.
- 5. The method of forming a semiconductor device according to claim 4, wherein said As<sup>+</sup> dopant implantation energy, dose, and tilt angle are approximately about 2 7 keV, 3E11 -

 $7E11 \text{ ions/cm}^2$ , and 5-10 degrees of tilt angle respectively; and for P<sup>+</sup> ion, implant energy, dose and tilt angle are approximately about 2-15 keV, 3E11-7E11 ions/cm<sup>2</sup>, and 5-10 degrees respectively.

- 6. The method of forming a semiconductor device according to claim 1, wherein said second implanted dopant comprises n- or p- type ions.
- 7. The method of forming a semiconductor device according to claim 6, wherein said second implanted n- type dopant is As<sup>+</sup> or P<sup>+</sup> ion.
- 8. The method of forming a semiconductor device according to claim 7, wherein said second  $As^+$  or  $P^+$  ion dopant implantation energy, dose, and tilt angle are approximately about 80-140 keV, 1E13-2E13 ions/cm<sup>2</sup>, and 0-15 degrees of tilt angle respectively.
  - 9. A method of forming a semiconductor device, the steps comprising:

forming a silicon dioxide layer on a silicon substrate;

forming a silicon nitride layer on said silicon dioxide layer;

forming isolation trench regions in said silicon substrate and removing said silicon nitride;

first implantation of As+dopant through said silicon dioxide layer;

second implantation of As<sup>+</sup> dopant through said implanted silicon dioxide layer to form wells; and

removing said implanted silicon dioxide layer and forming a gate dielectric layer over

said silicon substrate.

- 10. The method of forming a semiconductor device according to claim 9, wherein said silicon dioxide layer thickness is approximately about 25 °A 120 °A.
- 11. The method of forming a semiconductor device according to claim 9, wherein said first implanted As<sup>+</sup> dopant implantation energy, dose, and tilt angle are approximately about 2-7 keV, 3E11-7E11 ions/cm<sup>2</sup>, and 5-10 degrees of tilt angle respectively.
- 12. The method of forming a semiconductor device according to claim 9, wherein said second implanted As<sup>+</sup> dopant implantation energy, dose, and tilt angle are approximately about 80 140 keV, 1E13 2E13 ions/cm<sup>2</sup>, and 0 15 degrees of tilt angle respectively.
- 13. A method of forming a semiconductor device with improved threshold voltage stability, the steps comprising:

forming isolation trenches in a silicon substrate with steps comprising: forming silicon nitride over silicon dioxide stack on said silicon substrate; and selective removal of said silicon nitride;

forming a sacrificial implanted silicon dioxide layer by implanting first As<sup>+</sup> ions into said silicon dioxide layer;

forming n-well in silicon substrate by second implantation of As<sup>+</sup> ions; and removing said implanted silicon dioxide layer and forming a gate dielectric layer over said silicon substrate.

- 14. The method of forming a semiconductor device according to claim 13, wherein said silicon dioxide layer thickness is approximately about 25 °A 120 °A.
- 15. The method of forming a semiconductor device according to claim 13, wherein said first implanted As<sup>+</sup> dopant implantation energy, ion dose, and tilt angle are approximately about 2 7 keV, 3E11 7E11 ions/cm<sup>2</sup>, and 5 10 degrees of tilt angle respectively.
- 16. The method of forming a semiconductor device according to claim 13, wherein said second implanted As<sup>+</sup> dopant implantation energy, dose, and tilt angle are approximately about 80 140 keV, 1E13 2E13 ions/cm<sup>2</sup>, and 0 15 degrees of tilt angle respectively.